Amendments to the Specification

Please ADD the following heading and new paragraph on page 1 of the Specification, after the title:

-- CROSS REFERENCE TO RELATED APPLICATIONS

This application is a Division of co-pending application Serial No. 09/802,702, filed on March 9, 2001 by Arne W. Ballantine, et al., entitled METHOD OF REDUCING POLYSILICON DEPLETION IN A POLYSILICON GATE ELECTRODE BY DEPOSITING POLYSILICON OF VARYING GRAIN SIZE, the entire contents of which is incorporated by reference, and for which priority is claimed under 35 U.S.C. § 120. --

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently Amended) A method of forming a crystalline polysilicon gate electrode structure on a gate dielectric, comprising ~~the steps of~~:

depositing, on the gate dielectric, polysilicon crystals of substantially a first size; and

contiguously with the crystals of the first size, depositing directly thereon additional polysilicon crystals of substantially a second size.

2. (Original) The method according to claim 1, wherein:

the first crystal size is larger than the second crystal size.

3. (Original) The method according to claim 1, wherein:

the first crystal size is smaller than the second crystal size.

4. (Currently Amended) A method of forming a crystalline polysilicon gate electrode structure on a gate dielectric, comprising ~~the step of~~:

controlling a variation of at least one of temperature, pressure, and flow rate of a continuous flow of silane or related silicon precursor species while depositing polysilicon therefrom as crystals of correspondingly controlled grain size.

5. (Original) The method according to claim 4, wherein:

the variation is controlled in step-wise manner, to thereby form a multi-region polycrystalline silicon deposit comprising regions having crystals of respective grain sizes.

6. (Original) The method according to claim 5, wherein:

crystals deposited in a first region adjacent to the gate dielectric have a first grain size selected to maximize dopant activation near the gate dielectric and a second region that has

crystals of a second grain size deposited more distantly from the gate dielectric.

7. (Currently Amended) A method of forming a polycrystalline silicon structure in which crystal grain size varies as a function of depth, comprising ~~the step of~~:

controlling a variation of at least one of temperature, pressure, and flow rate of a silane gas while depositing silicon therefrom, to thereby control the crystal grain size as a function of depth in the deposited polysilicon structure.

8. (Original) The method according to claim 7, wherein:

the polysilicon structure comprises a plurality of regions having respective grain sizes.

9. (Original) The method according to claim 8, wherein:

the polycrystalline silicon structure is a gate electrode formed on a gate dielectric, and comprises a first region having a first crystal grain size and a second region formed thereon and having a second grain size.,

wherein the first and second grain sizes are selected to maximize dopant activation in the first region and to achieve a specific resistance in the second region.

10. (Original) The method according to claim 9, further comprising:

a third region formed on the second region and having crystals of a third grain size, to further tailor the resistance of the gate conductor structure.

11. (Original) The method according to claim 8, wherein:

the electrical resistance of the deposited silicon varies inversely with the controlled pressure.

12. (Currently Amended) The method according to claim 7, <u>further</u> comprising ~~the further step of~~:

providing a controlled flow of a dopant gas during a selected portion of the step of depositing polysilicon, to thereby enable selected doping or counter-doping of a portion of the deposited polysilicon.

13. (Original) The method according to claim 12, wherein:

the dopant gas is selected to provide one of a p-type or an n-type doping during a final portion of the step of depositing polysilicon.

14. (Currently Amended) The method according to claim 7, further comprising ~~the further step of~~:

forming a layer rich in carbon atoms at a selected stage of the silicon deposition.

15. (Currently Amended) The method according to claim 7, further comprising ~~the further step of~~:

forming a layer of silicon-germanium at a selected stage of the silicon deposition.

16. (Original) The method according to claim 7, wherein:

the variation is controlled to deposit the polysilicon so that the crystal grain size varies monotonically during the deposition of the polysilicon.

Claims 17-22 (Cancelled)

23. (New) A CMOS transistor, comprising:

a dielectric film;

a gate conductor on the dielectric film,

wherein the gate conductor includes a region of polycrystalline silicon,

said region of polycrystalline silicon having a continuously varying grain size as a function of a distance measured from a surface of the dielectric film.

24. (New) The CMOS transistor of claim 23, wherein said continuously varying grain size decreases continuously as a function of the distance measured from a surface of the dielectric film.

25. (New) The CMOS transistor of claim 23, wherein said continuously varying grain size increases continuously as a function of the distance measured from a surface of the dielectric film.

Application No.: To Be Assigned

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REMARKS/ARGUMENTS

Each of the presently pending claims 1-16 and 23-25 in this divisional application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Please charge IBM Deposit Account No. 09-0456, under Order No. 21806-00113-US1 from which the undersigned is authorized to draw.

Dated: July 11, 2003

Respectfully submitted,

By Larry J. Hume

Larry J. Hume

Registration No.: 44,163

CONNOLLY BOVE LODGE & HUTZ LLP
1990 M Street, N.W., Suite 800
Washington, DC 20036-3425
(202) 331-7111
(202) 293-6229 (Fax)
Attorney for Applicant

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